

LOW POWER DYNAMIC COMPARATOR DESIGN USING VARIABLE RESISTOR

A Thesis submitted in partial fulfilment of the Requirements for the degree of

Master of Technology

In

Electronics and Communication Engineering

Specialization: VLSI Design & Embedded System

By

Nitin Jain

Under the Guidance of

Prof. M Nurul Islam



Department of Electronics and Communication Engineering
National Institute of Technology Rourkela Rourkela, Odisha,
769 008, India



**DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
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This is to certify that the work in the thesis entitled “**Design of low power dynamic comparator using voltage variable resistor in discharging path**” by **Nitin Jain** is a record of an original research work carried out by him during 2014 - 2015 under my supervision and guidance in partial fulfilment of the requirements for the award of the degree of Master of Technology in Electronics and Communication Engineering (VLSI Design & Embedded System), National Institute of Technology, Rourkela. Neither this thesis nor any part of it, to the best of my knowledge, has been submitted for any degree or diploma elsewhere.

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Dept. of Electronics and Communication Engg.

National Institute of Technology

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Nitin Jain

28th May 2015

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Nitin Jain

neetjain3@gmail.com

ABSTRACT

In today's reality, where claim for versatile battery functioned gadgets is expanding, a noteworthy plunge is given in the direction of low power approaches for rapid applications. To reduce the feature size is the cause to reduce the power. The comparator is one of the most versatile circuits in analog circuit design. It serves as an input stage of most of the ADCs. The comparator has noteworthy effect on the execution of the objective application which depends on the architecture and form of it. In this thesis, a clock based comparator is analysed in terms of average power dissipation, delay power-delay product (PDP). An investigation of modified double tail dynamic comparator has been carried out using post layout simulations. Based on the analytical expressions, a new comparator circuit that consumes less power has been proposed. Simple modification has been done by adding MOS transistor that works as voltage variable resistor (MOSFET in triode region) to reduce power. The delay of the proposed circuit is also improved as the voltage variable resistor increases the differential voltage in pre amplifier stage. Post layout simulation of the design in 90nm CMOS technology is presented. The average power dissipations of the proposed comparator at two different supply voltages which is 0.6 and 1.2 V are 0.842 μ W and 2.68 μ W respectively. The clock frequency at which circuit gives proper output of the proposed circuit goes up to 1.33GHz and 1GHz at supply voltages of 1.2V and 0.6V.

MOTIVATION

In today's world, where claim for portable battery functioned devices is increasing, a major plunge is given in the direction of low power approaches for high speed applications. With the quick growth of microchip technology engineering typically portable electronics systems, which is wireless communication devices, battery-powered medical devices etc. In all these application battery life is one of the most important factors. So need of low power and low voltages is very essential. IC's cost can also reducing by using thicker oxide layer or higher supply voltages Normally, In the IC's where analog to digital convertor or digital to analog convertor plays an important role, low power and low voltage comparator is very essential and necessary thing. Comparator is the important part of ADC's and also consumes large power in device. It is essential or primary concern to achieve low power and high speed comparator. By and large, low-voltage circuit outline is alluring to diminish the quantity of battery cells for reasons of low weight and little framework size.

Literature survey:

- Samaneh Babayan-Mashhadi, Reza Lotfi

. In this paper describe the analytical way to reduce the delay of double-tail dynamic comparator. This expression results a trade-off between the power and the delay. A novel technique is proposed with used a regenerated clocked based pre-amplifier is used. This regenerated clocked based pre-amplifier makes positive feedback in the circuit so that delay of the circuit is reduced up to great extant. .Post layout simulation is done in 180 nm cmos technology.

- Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger

If offset voltage of the comparator is static then it is easily remove but if it is random than it is unpredictable. In this paper describe that random offset voltage present in the circuit due to internal mismatch of the circuit. It tells that due to random offset voltage operating point of the transistor is varying. According to this a novel balanced method is offered to enable the estimation of operating points of transistors in a dynamic comparator. If the operating point is find then the calculation of the offset voltages is very easy. To approve the result 25nm and 40nm technique is used.

- Tsuguo Kobayashi, Kazutaka Nogami, Tsukasa Shirotori, and Yukihiro Fujimoto

In this paper two novel technique is describes to reduce the power in the circuit. One of them is static power saving input buffer (SPSIB)which is reduce the dc current by making TTL high input level. The other technique is a current-controlled latch sense amplifier. It is reduce the power without affecting the delay by using stopping sense current automatically.

- A. Nikoozadeh and B. Murmann

In this paper describes the causing and removing technique of offset voltage in regenerative latch comparator. It is also describes that how offset voltage depends on load capacitor mismatch. Two different analytical models are presented and post layout simulation done in 180 nm cmos technology.

- B. J. Blalock' H. W. Liz P.E. Allen S.A. Jackson

This paper describes that using body-driving technique simply low voltage analog circuit design. Based on this technique a new topology is presented. In this technique a class AB amplifier is presented along with topologies for amplifiers and a four quadrant multiplier.

- Bernhard Wicht, , Thomas Nirschl, and Doris Schmitt-Landsiedel

In this paper also investigates the offset voltage in terms of input dc level, supply voltage, transistor sizing, and temperature. The data dc level ends up being generally critical. Additionally, a scientific expression for the detecting deferral is determined which shows low affectability on the information dc inclination voltage.

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CHAPTER 1:

INTRODUCTION

1.1 Background Motivation:

In today's world, where claim for portable battery functioned devices is increasing, a major plunge is given in the direction of low power approaches for high speed applications. With the quick growth of microchip technology engineering typically portable electronics systems, which is wireless communication devices, battery-powered medical devices etc. In all these application battery life is one of the most important factors. So need of low power and low voltages is very essential. IC's cost can also reducing by using thicker oxide layer or higher supply voltages Normally, In the IC's where analog to digital convertor or digital to analog convertor plays an important role, low power and low voltage comparator is very essential and necessary thing. Comparator is the important part of ADC's and also consumes large power in device. It is essential or primary concern to achieve low power and high speed comparator. In general, low-voltage circuit design is desirable to reduce the number of battery cells for reasons of low weight and small system size.

This drop in power can be attained by moving to reduced feature size methods. The comparator is one of the most versatile circuits in analog circuit design. It serves as an input stage of most of the ADCs. The comparator has noteworthy effect on the execution of the objective application which relies on upon the construction modeling and type of it. Comparator's input signal range and corresponding input offset voltage and the delay directly affects ADC's resolution and speed. The overall performance of the device will greatly be affected as we concentrate on the process variations, smaller feature size processes and other non-ideal ties. Contingent upon nature, usefulness and inputs, comparators are sorted into diverse kind's i.e. nonstop and discrete time comparators voltage and current comparators, and so on. Different utilizations of comparators are signal discovery and neural systems capacity era and so on.

1.2 Application of Comparator:

- (1) **Threshold Detector:** Threshold detector is the vital application of the comparator. It is works as a voltage switch, difference between the normal voltage switch and voltage detector that output state of the threshold detector is not dependent on the input of the detector, but instead by the voltage drop across its input terminals

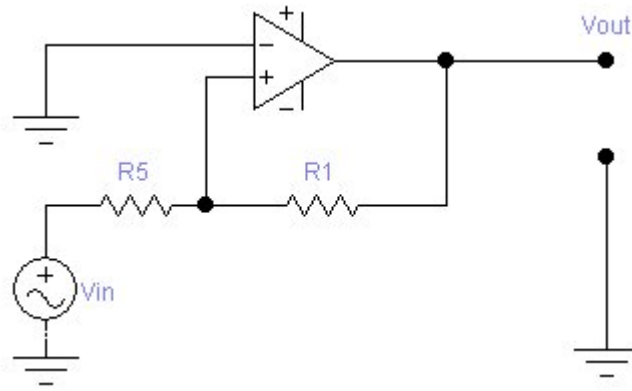


Fig1.1 Threshold Detector

$$V_a = \frac{R_1}{R_1 + R_5} V_{in} + \frac{R_5}{R_1 + R_5} V_{TH Rout}$$

(2) **Zero Crossing Detector:**

Zero crossing detectors are another application of the comparator which is widely used. It is used zero crossing of AC signals with make one terminal level set as a zero or make as a reference terminal. If input voltage is positive then output value is also positive and if input voltage is negative then output voltage is also negative.

(3) **Relaxation Oscillator:**

By changing or make a small modification in the Schmitt trigger a relaxation oscillator is formed. Create the negative feedback using RC network in the inverting terminal of Schmitt trigger relaxation oscillator is formed.

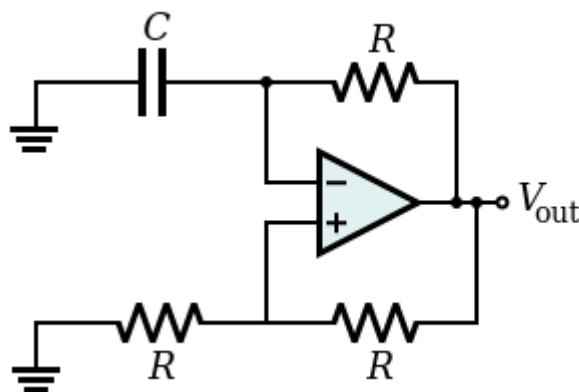


Fig 1.2 Relaxation oscillator

1.3 Previous Work in Comparator:- In view of its stringent requirement in the design of analog

and mixed mode circuits, a wide variety of comparator has been reported in literature [13]. In order to make a high speed and low power comparator, preamplifier based comparator is used as shown in Fig. 1(a). But due to static mismatches such as threshold voltage V_{Th} and $\mu_n C_{ox}$, variation becomes a critical issues in such comparators [7, 8] [14]. To overcome these problems dynamic comparator has proposed in literature [10, 11]. Fig. 1(b) shows a circuit schematic of such a dynamic comparator. Due to this Outa or Outb node discharge very rapidly causing a little amplification in the difference of input voltage. Although it has the advantage of low power dissipation but it suffers severely from dependency of input evaluation on common-mode input voltage (V_{cm}). It is also less attractive to wide common mode range such as ADCs [12] [14]. In order to avoid these drawbacks, double tail dynamic comparator [7] is used a different tail transistor for both pre-amplifier and latch stage. Cross coupled inverters also provide an excellent shielding between input and output, resulting a reduced value of kickback noise [12][13].

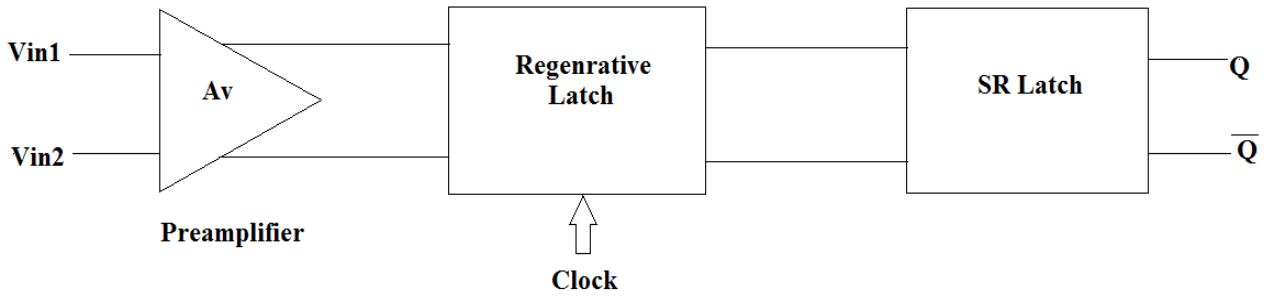


Fig 1.3 Pre-amplifier Based Comparator

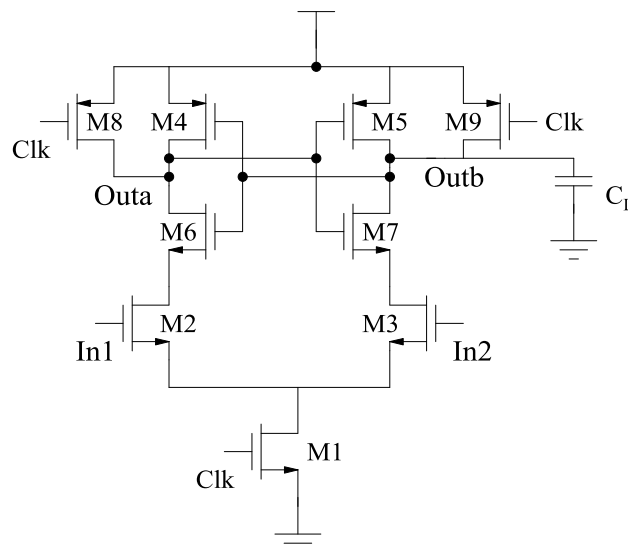


Fig. 1.4 Conventional Dynamic Comparator

In this literature we will discuss that a small change in circuitry of pre-amplifier stage in dynamic comparator. Placing voltage variable resistor in the discharging path of pre-amplifier stage effect both power consumption and the delay of the circuit. We reduced power of comparator up to a great extent as well as delay of the circuit is also reduced up to some extent.

1.4 This Organization:-

This thesis provided low power and high speed comparator using voltage variable resistor in the discharging path. Content of thesis as follow

Chapter 1 Introduction of Comparator

Chapter 2 This chapter defines the basic characteristics and the operation of the comparator. In this chapter characteristic like DC Gain, Slew Rate, Propagation Delay, Offset Voltages, ICMR etc define. This chapter tells that how offset voltage and range of ICMR effects the operation of the comparator.

Chapter 3 This chapter define the conventional dynamic comparator. In this chapter working of the comparator, power calculation, delay calculation etc. From the power calculation it can be easily seen that trans-conductance (g_m) of transistor in preamplifier plays an important role in power consumption. According to this a new dynamic comparator has been proposed. In proposed Comparator a small modification implemented in pre-amplifier stage of dynamic comparator so reduction of power up to a great extant.

Chapter 4 Due to trans-Conductance (g_m) is greatly effects the power consumption of the comparator a proposed Double-Tail Dynamic Comparator has been define in this chapter. In this literature we will discuss that a small change in circuitry of pre-amplifier stage in dynamic comparator. Placing voltage variable resistor in the discharging path of pre-amplifier stage effect both power consumption and the delay of the circuit. We reduced power of comparator up to a great extent as well as delay of the circuit is also reduced up to some extent. In this chapter also shows the percentage improvement in terms of power consumption, delay, power-delay product (PDP). The average power dissipations of the proposed comparator at supply voltages of 1.2 and 0.6 V are 2.68 μ W and 0.842 μ W respectively. The maximum clock frequency of the proposed circuit goes up to 1.33GHz and 1GHz at supply voltages of 1.2V and 0.6V.

Chapter 5 It shows the conclusion and the future work.

CHAPTER 2:

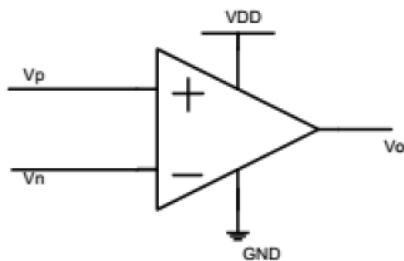
FUNDAMENTALS OF COMPARATOR DESIGN

2.1 BASIC CMOS COMPARATOR

Fig1.1 shows the basic cmos based comparator

Definition: By the name comparator is used to compare two analog signal and according to this it gives output weather logic 0 or logic 1.

A comparator is a device that compares currents or voltages and outputs comes in digital which is very larger compare to the input voltages. It has two input terminals V_P and V_N and one digital output V_O . The output comes in ideally



$V_P < V_N$ then $V_O = V_{SS} = \text{logic 0.}$

$V_P > V_N$ then $V_O = V_{DD} = \text{logic 1.}$

Fig. 2.1 Basic CMOS Comparator

In Fig 1.1 shows 1 bit comparator. V_P and V_N are two input and V_O is the output. In $V_P < V_N$ output comes logic 0 and if $V_P > V_N$ then output comes logic 1. If a positive voltage applied at the positive terminal then output goes to high logic. This high logic or upper limit is called V_{OH} . If a positive voltage applied at the negative terminal then output goes to low logic. This low logic or lower limit is called V_{OL} .

Schematically, In the comparator there are mainly three stages. First one is the input stage which is high gain differential stage. It is use to amplifies the differential input and reject the common mode input. Second stage is the decision making stage is use to convert one logic level to another with in very less time. The final stage is the output stage or the buffer stage. It is make the output of comparator to high logic or ground so it is easily drive the output.

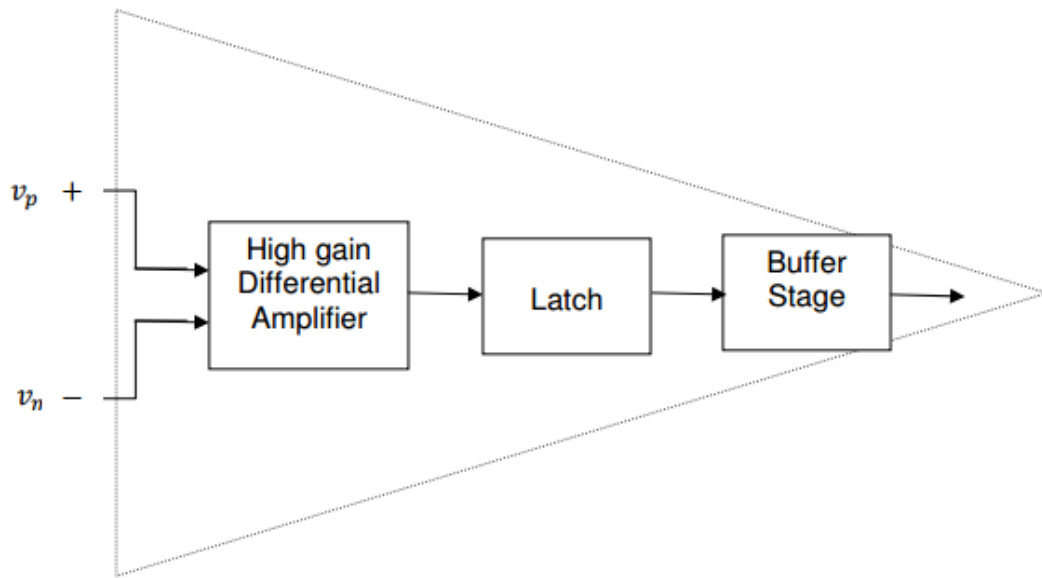


Fig 2.2 Schematic of Comparator

The output of the comparator ideally is given in fig XX. Offset voltages is come due to the delay and some non-idealist of the comparator. If the value of the offset voltages is constant then it is easily removed but if its value is changes due to mismatch then it creates problem and eliminating of offset voltages is also difficult.

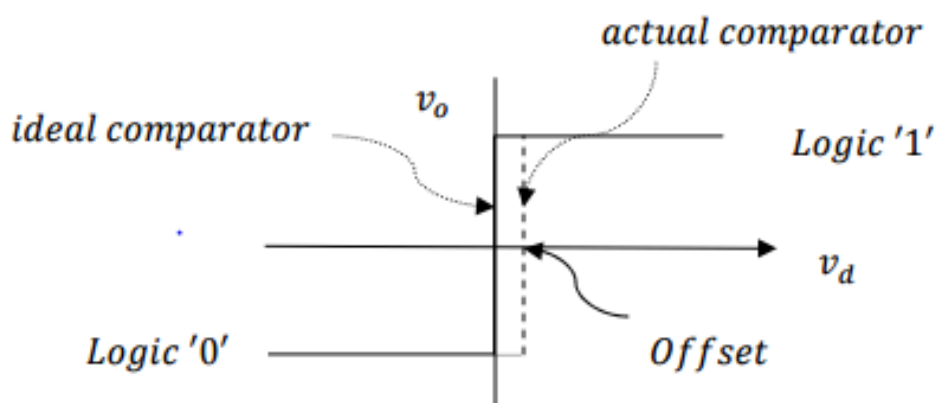


Fig 2.3 Output of the Ideal Comparator

The working of the OPAMP and comparator is similar in the sense that comparator is probable to react only to the differential inputs and disregard the common mode component. However, Comparator and OPAMP is completely different in many ways and also the working of both device is also different. Normally OPAMP is always used as a linear mode circuit and operated in negative feedback region. Whereas the comparator is always operated in positive feedback or in open loop condition. So the design strategy of the comparator and OPAMP is completely different. OPAMP has again another issue that is stability issue, and to remove it used compensation technique is used. In comparator there is no any problem of stability due to it need high bandwidth. The comparator design is free from this constraint, and therefore can aim and achieve much higher bandwidth.

2.2. CHARACTERISATION OF COMPARATOR:-

A comparator has basically two types of characteristics.

- (1). Static Characteristics
- (2). Dynamic Characteristics

2.1. A. Static Characteristics:-

When the difference between positive and negative terminal is positive then the output of the comparator is high logic level (V_{OH}), and when difference is negative then output is low (V_{OL}). In Fig shows the ideal characteristic of the comparator. When the value of V_H is greater than value of V_N then the output goes to the V_{OH} . When the value of V_H is smaller than value of V_N then the output goes to the V_{OL} . However, It is not possible due to it takes a small time to sense the input and gives the output and also it takes some differential voltage to drive the comparator and producing the output.

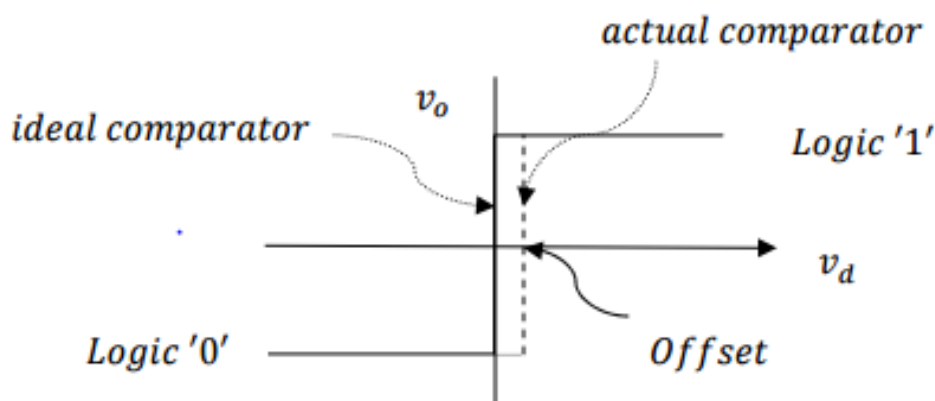
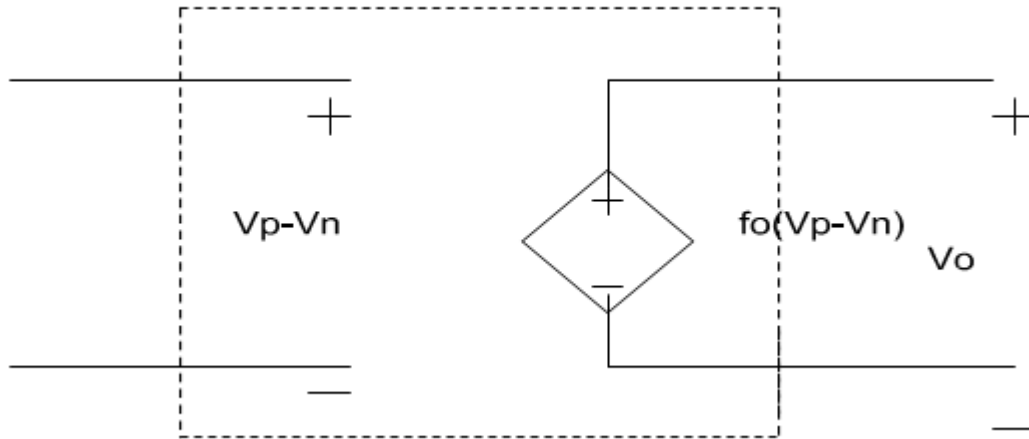


Fig 2.4 Static Characteristics of Ideal and Practical Comparator



For $V_P - V_N = V_{OH}$ When $V_P - V_N > 0$

$V_P - V_N = V_{OL}$ When $V_P - V_N < 0$

Fig 2.5 Small Signal Model of Comparator

V_{OS} is stand for input offset voltage which is the another non ideal characteristics of the comparator. Fig 2.4 shows the effect of the offset voltage in the characteristics of the comparator. Without offset voltage when input voltage level changes at that point the logic level changes but due to offset voltage it is changes after some time or with some delay. If it is fixed then it would ot create problem but due to randomly varies it create problem Figure 2.4 shows offset in the transfer curve for a comparator, with the circuit model including an offset generator shown in Fig.2.5

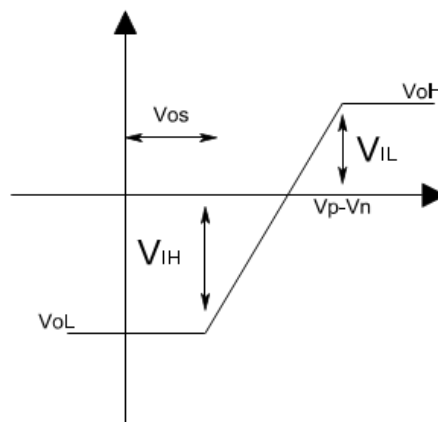


Fig 2.6(a)

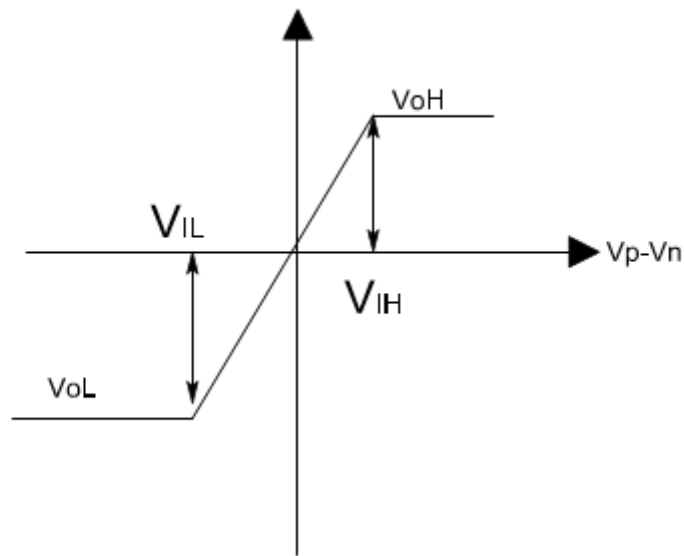


Fig2.6 (b)

Fig 2.6 Transfer characteristics of Practical and Ideal Comparator

ICMR is the property of the comparator which implies the range of the input voltage at which comparator works in proper way. When all the comparator in saturation region then the comparator works in proper way. So ICMR (Input Common Mode Range) tells that up to which input voltage output comes in proper way.

Noise is also another uncertainty or characteristics of the comparator. Due to this jitter and other non-ideal will coming in the circuit.

2.3. Dynamic Characteristics:-

Dynamic characteristics comprise the delay of the circuit, Power dissipation and power delay product of the comparator. The dynamic qualities of the comparator incorporate both little flag and vast sign conduct. We don't have the foggiest idea, as of right now, to what extent it takes for the comparator to react to the given differential data. The trademark postpones between info excitation and yield move is the time reaction of the comparator. Figure 2.7 delineates the reaction of a comparator to a data as a component of time. Note that there is a postponement between the info excitation and the yield reaction. This time distinction is known as the spread postponement time of the comparator. It is a critical parameter since it is regularly the pace impediment in the change rate of an A/D Converter.

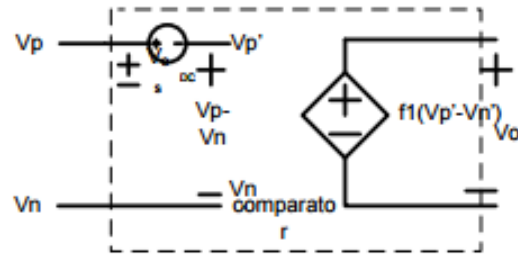


Fig 2.7 Small Signal model with input offset voltage

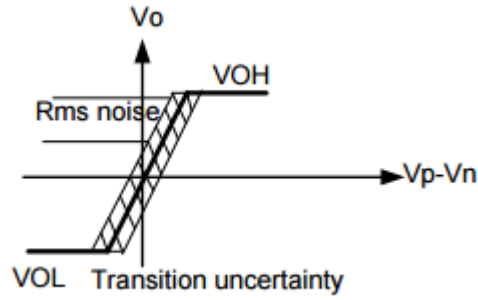


Fig 2.8 Transition include noise

The spread deferral time in comparators for the most part differs as an element of the adequacy of the data. A bigger info will bring about a littler deferral time. There is a maximum farthest point at which a further increment in the data voltage will no more influence the postponement. This method of operation is called slewing or slew rate. The little flag progress is described by the recurrence reaction of the comparator. A straightforward model of this conduct accept that the differential voltage pick up, A_v , is given as

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1} \quad (2.1)$$

Where $A_v(0)$ is the dc increase of the comparator.

Give us a chance to accept that the base change of voltage at the info of the comparator the determination of the comparator. We will characterize this base data voltage to the comparator as

$$V_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_v(0)} \quad (2.2)$$

For a stage information voltage, the yield of the comparator demonstrated by Eq. (2.1) ascents (or falls) with a first-order exponential time reaction from VOL to VOH or (VOH to VOL). On the off chance that V_{in} is bigger than $V_{in}(\min)$, the yield rise or fall time is speedier. At the point when $V_{in}(\min)$ is connected to the comparator, we can compose the accompanying mathematical statement

$$\frac{V_{OH} - V_{OL}}{2} = A_V(0)[1 - e^{-T_P/\tau_C}]V_{in}(\min) = A_V(0)[1 - e^{-T_P/\tau_C}](\frac{V_{OH} - V_{OL}}{A_V(0)}) \quad (2.3)$$

Thusly, the engendering deferral time for an information venture of $V_{in}(\min)$ can be communicated as

$$t_P(\max) = \tau_c \ln(2) = 0.693\tau_c \quad (2.4)$$

Thusly, the engendering deferral time for an information venture of $V_{in}(\min)$ can be communicated as

$$t_P = \tau_c \ln(\frac{2k}{2k-1}) \quad (2.5)$$

$$\text{where } k = \frac{V_{in}}{V_{in}(\min)} V_{in}. \quad (2.6)$$

Clearly, the more overdrive connected to the data of this comparator, the littler the proliferation postponement time. As the overdrive increments to the comparator in the end the comparator enters a vast sign method of operation. Under extensive sign operation, a large number rate cut off will happen because of restricted current to charge or release capacitors.

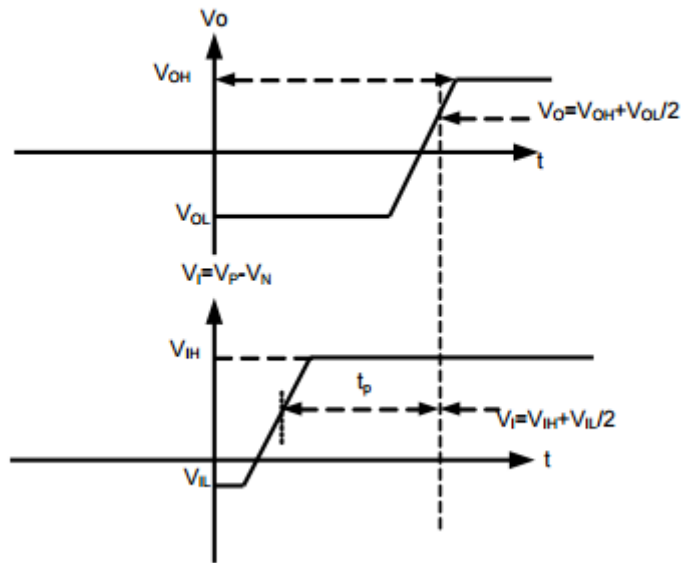


Fig.2.9 Calculation of Propagation Delay for inverter

In the event that the proliferation deferral time is controlled by the large number rate of the comparator, then this time can be composed as

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2.SR} \quad (2.7)$$

For the situation where the engendering time is controlled by the huge number rate, the most vital variable to lessening the spread time is expanding the sinking or sourcing capability)of the comparator. A square chart of an elite comparator is indicated in fig.2.8

2.2. Block diagram of General Type CMOS Comparator:

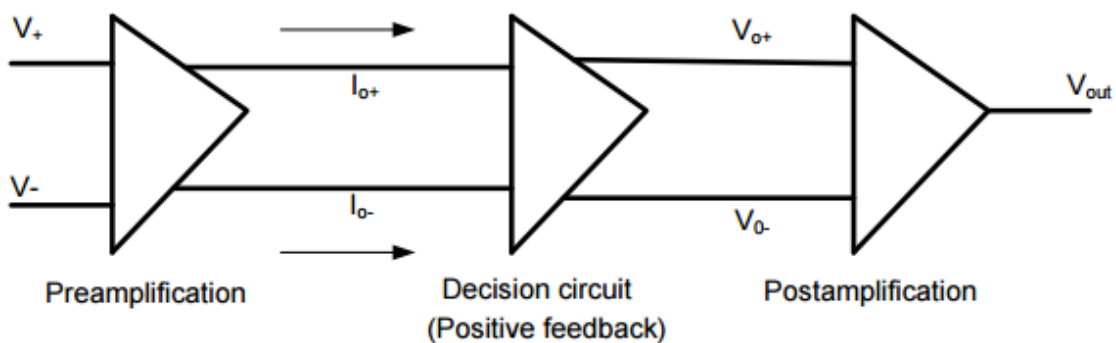


Fig 2.10 Comparator using voltage amplifier

There are three stages in this comparator .The preamplifier, a positive criticism or choice

making stage and a yield cradle stage. The preamp stage intensifies the data sign to progress the comparator affectability (i.e. expands the base info signal with which the comparator can settle on a choice) and secludes the data of the comparator from changing clamor originating from the positive input stage i.e. kick back commotion impact. This clamor impact is lessened by utilizing Hooked based comparator (examined in section 4). The positive criticism stage is utilized to figure out which of the data sign is bigger. The yield support opens up this data and yields an advanced sign. Outlining a comparator can start with considering information regular mode reach, power dispersal, engendering deferral and comparator pick up. We will build up an essential comparator outline utilizing a method like the essential operation amp.

2.4. OFFSET ERROR VOLTAGES AND CURRENTS:-

The perfect operational speaker demonstrated in Fig. 2.11 is impeccably adjusted, that is, $V_o = 0$ when $V_1 = V_2$. A genuine operational speaker shows an unbalance created by a confuse of the info transistors. This bungle brings about unequal inclination streams coursing through the info terminals, furthermore obliges that an info counterbalance voltage be connected between the two data terminals to parity the enhancer yield. In this area the DC slip voltages and streams that can be measured at the information and yield terminal

Input Bias Current: The data predisposition current is one-a large portion of the total of the different streams entering the two info terminals of an adjusted enhancer as indicated in Fig.2.9(a) the data predisposition current is $I_B = (I_{B1} + I_{B2})/2$ when $V_o = 0$.

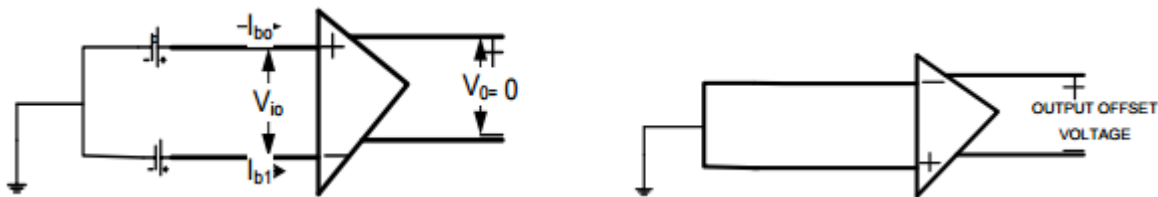


Fig. 2.11 Calculation of input and output offset voltage

Input Offset Current:- The data counterbalance current is the distinction between the different streams entering the information terminals of an adjusted enhancer. As demonstrated in Fig, 2.11, we have $I_{io} = I_{B1} - I_{B2}$ when $V_a = 0$.

Input Offset Voltage : The data counterbalance voltage V_{ia} is that voltage which must be connected between the data terminals to adjust the speaker, as demonstrated in Fig. 2.11.

Output Offset Voltage: The yield counterbalance voltage is the contrast between the dc voltages present at the two yield terminals (or at the yield terminal and ground for a speaker

with one yield) when the two info terminals are grounded (Fig. 2.11).

Power Supply Rejection Ratio:- The force supply dismissal proportion (PSRR) is the proportion of the change in information balance voltage to the relating divert in one force supply voltage, with all remaining power supply voltage steady.

2.5. Improving the Performance of open loop comparators:-

There are two territories in which the execution of an open-circle, high-pick up comparator can be enhanced with minimal additional exertion. These territories are the info balance voltage and a solitary move of the comparator in a boisterous domain. The principal issue can be illuminated via auto focusing and the second can be explained by the presentation of hysteresis utilizing a bistable circuit.

These two methods will be inspected in the accompanying.

Auto zeroing Techniques:-

Data counterbalance voltage can be an especially troublesome issue in comparator outline. In exactness applications, for example, high-determination ADC's converters, extensive data balance voltages can't go on without serious consequences. While deliberate balance can almost be killed with legitimate outline (however still influenced by procedure varieties), arbitrary balances still remain and are unusual. Luckily there are systems in MOS innovation to uproot an extensive part of the info counterbalance utilizing counterbalance scratch-off methods. These methods are accessible in MOS in view of the about unending info resistance of MOS transistors. This trademark permits long haul stockpiling of voltages on the transistor's entryway. Therefore, counterbalance voltages can be measured, put away on capacitors, and summed with the data to scratch off the counterbalance.

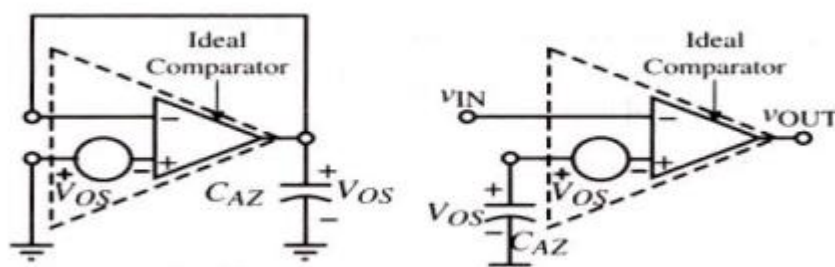


Fig. 2.12 Technique to remove the offset voltage

2.12 Comparator solidarity pick up setup putting away the counterbalance on auto zero capacitor CAZ amid initially a large portion of the auto zero cycle. 2.12 Comparator in open-circle arrangement balance scratch-offs accomplished at the non-modifying data amid the

second 50% of the auto zero cycle. A model of a comparator with an info counterbalance voltage is indicated in Fig (2.12). A known extremity is given to the situated voltage for comfort. Neither the quality nor the extremity can be anticipated as a general rule. Figure (2.12) demonstrates the comparator associated in the unitygain setup so that the information balance is

accessible at the yield. All together for this circuit to work appropriately, it is important that the comparator be stable in the solidarity pick up arrangement.

This suggests that just self-remunerated high-pick up enhancers would be suitable for auto focusing. One could utilize the two stage, open-circle comparator however a remuneration circuit ought to be exchanged into the circuit amid auto focusing. In the last operation of the auto zero calculations CAZ is put at the information of the comparator in arrangement with Vos. The voltage crosswise over CAZ adds to Vos, bringing about zero volts at the no modifying information of the comparator. Since there is no de way to release the auto zero capacitor, the voltage crosswise over it remains uncertainly (in the perfect case). In reality, there are spillage ways in shunt with CAZ that can release it more than a time of time. The answer for this issue is to rehash the auto zero cycle occasionally.

A common sense usage of a differential-data, auto focused comparator is [1] indicated Fig.(2.11.a). The comparator is displayed with a balance voltage source as some time recently. Figure (2.11.b) demonstrates the condition of the circuit amid the first period of the cycle when 1 is high. The counterbalance is put away over

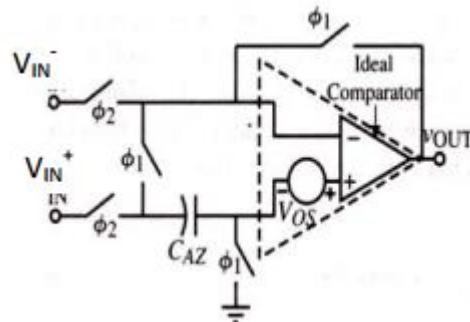


Fig. 2.13 Cancellation of offset voltage

Delay of the circuit depends on the time taken by circuit to produce the output when the input is applied. Ideally the value of the delay is zero, but practically it has some finite value. Propagation delay of comparator is time between 50% input to 50% output.

$$T_p = \Delta T = \frac{\Delta V}{SR} = \frac{(V_{OH} - V_{OL})}{2SR}$$

Slew Rate (SR):

Slew rate is defined as the rate of change of output voltage with respect to time.

$$S.R = \frac{dV_{OUT}}{dt}$$

Slew Rate of the comparator should be high for the normal operation of the comparator. Slew rate comes from the relationship.

$$I = C \frac{dV}{dT}$$

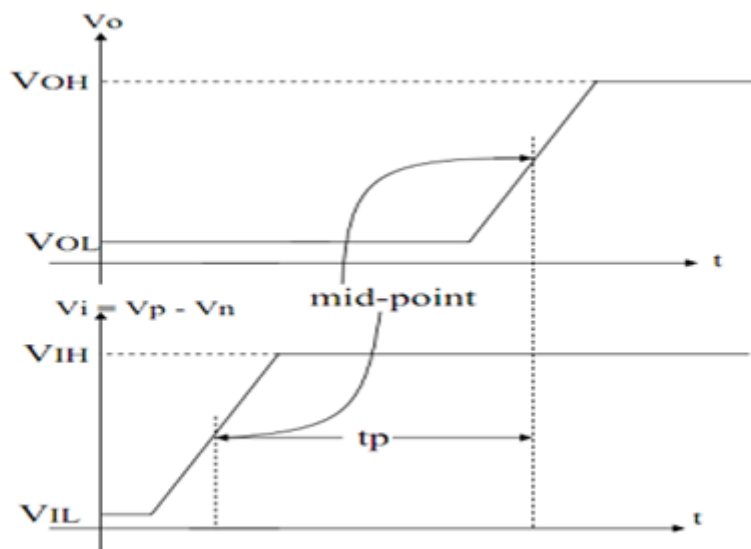


Fig 2.14 Propagation Delay of the Comparator

Chapter3.

CLOCKED BASED DOUBLE-TAIL DYNAMIC COMPARATOR

3.1 Introduction: In order to make a high speed and low power comparator, preamplifier based comparator is used. But due to static mismatches such as threshold voltage V_{Th} and $\mu_n C_{ox}$, variation becomes a critical issues in such comparators [7, 8] [14]. To overcome these problems dynamic comparator has proposed in literature [10, 11]. Although it has the advantage of low power dissipation but it suffers severely from dependency of input evaluation on common-mode input voltage (V_{cm}). It is also less attractive to wide common mode range such as ADCs [12] [14]. In order to avoid these drawbacks, double tail dynamic comparator [7] is used a different tail transistor for both pre-amplifier and latch stage. Cross coupled inverters also provide an excellent shielding between input and output, resulting a reduced value of kickback noise [12][13].

This chapter define the conventional dynamic comparator. In this chapter working of the comparator, power calculation, delay calculation etc. From the power calculation it can be easily seen that trans-conductance (g_m) of transistor in preamplifier plays an important role in power consumption. According to this a new dynamic comparator has been proposed. In proposed Comparator a small modification implemented in pre-amplifier stage of dynamic comparator so reduction of power up to a great extant.

Fig.3.1 shows the schematic diagram of the clocked based dynamic double-tail comparator.

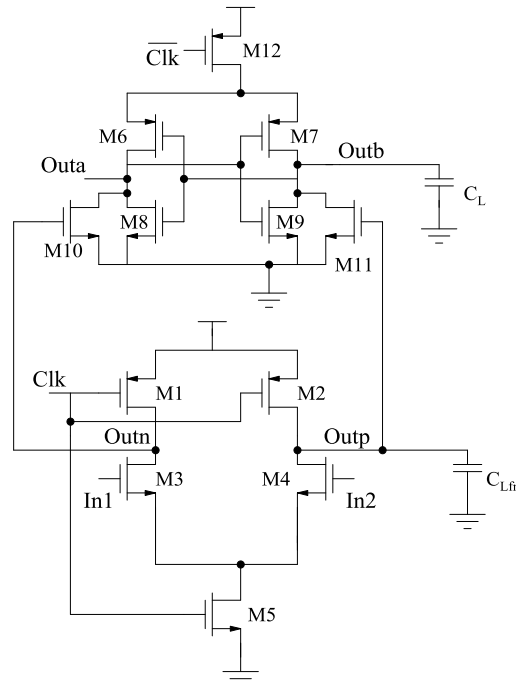


Fig. 3.1. Schematic diagram of the conventional double-tail dynamic comparator

3.2 Operation of the conventional circuit:

The operation of proposed circuit as follows (see Fig. 3.1). During the reset phase (i.e. $\text{clk}=0$) in preamplifier stage both pMOS, M1 & M2 are in conducting stage and pulls the node outp & outn to V_{DD} . The M5 nMOS is in cut-off mode, so there is no path to discharge for both outp & outn. Now in latch stage M12 is connected to V_{DD} , so the whole latch is in non-conducting phase and due to M10 and M11 outa and outb node are connected to ground.

During the decision-making phase (i.e. $\text{clk}=V_{DD}$) both pMOS come in cut-off stage, and there is no direct connection between V_{DD} and outp and outn nodes. So now outp and outq nodes start discharging according to the inputs IN1 & IN2. If $\text{IN1} > \text{IN2}$ then outp node will discharge rapidly compared to outq node. This voltage difference goes to the latch stage so at any instant M11 comes in cut-off stage while at this time M12 is in conducting stage, so outp node connected to the ground but outp node now charging from the V_{DD} . So using latch regeneration one node goes to V_{DD} , and another goes to ground. Cross coupled inverters also provides an excellent shielding between input and output, resulting in the reduced value of kickback noise [10].

Fig.3.2 shows the output of the double tail dynamic comparator. In the fig. it can be easily seen that In evaluation phase both outp and outn node discharge and according to this decision making phase started. So one of them outa and outb node goes to high and another remain in same condition.

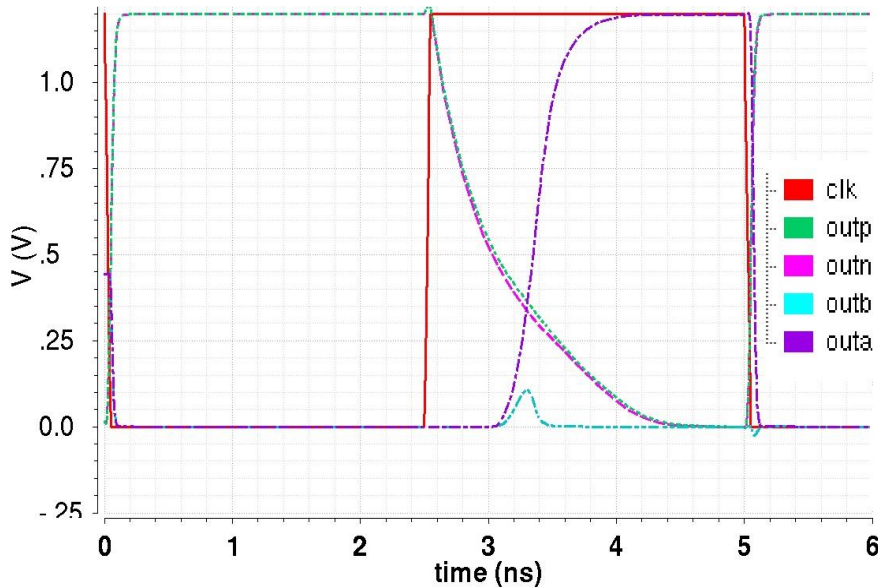


Fig. 3.2 Transient simulations of the proposed double-tail dynamic comparator. $V_{DD}=1.2\text{ V}$, $\Delta V_{in} = 5\text{ mV}$

3.3 Power Analysis:

Power of the comparator hold two main part dynamic power and static power.

$$P_{Total} = P_{Dynamic} + P_{Static} \quad (3.1)$$

Static power analysis: Static power is given by

$$P_{Static} = I_{Leakage} * V_{DD} \quad (3.2)$$

Dynamic power analysis: Dynamic power consists of two part switching power and short circuit power.

$$P_{Dynamic} = P_{Switching} + P_{ShortCircuit} \quad (3.3)$$

Short circuit power $P_{Short\ circuit}$ comes into the picture when clock is switch between either 0 to V_{DD} or V_{DD} to 0 and its value is calculated from [11].

$$P_{Short} = \frac{K}{12} (V_{DD} - V_{Thn})^3 \frac{\tau}{T} \quad (3.4)$$

Where K is the process parameter, τ is the rise time or fall time of clock signal, T is the time period of clock. Switching power $P_{Switching}$ is a transient power and it is given by

$$P_{Switching} = \int_0^T V_0(t) * I_0(t) \quad (3.5)$$

$$Power_{avg} = \frac{1}{T} \int_0^T V_{DD} I_{supply} dt = f_{clk} \cdot V_{DD} \cdot \int_0^T I_{supply} dt \quad (3.6)$$

Now, in order to calculate the power dissipation during the decision-making phase, we notice that I_{supply} is actually the drain current of M5 (see Fig. 3), hence we rewrite equation (3.6) by inserting the time-variant drain current of M5 according to Tsividis model [11].

$$Power_{avg} = f_{clk} V_{DD} I_{sp5} \int_{t_0}^{t_p} \ln^2 \left(1 + \exp \left(\frac{V_{DD} - V_{out}(t) - |V_{thp}|}{2n\phi_t} \right) \right) - \ln^2 \left(1 + \exp \left(\frac{V_{DD} - V_{out}(t) - |V_{thp}| - n(V_{DD} - V_{out}(t))}{2n\phi_t} \right) \right) dt \quad (3.7)$$

The integration is performed from the time that regeneration starts (at time t_0) until the end of the regeneration (t_p). In this equation, output voltages are functions of time. In [11] it has been proved that the difference voltage of latch outputs ($V_{outa}-V_{outb}$) changes in a logarithmic manner during the time as follows.

$$\Delta V_{out} = V_{outp} - V_{outn} = \Delta V_0 \exp(G_m t / C_{Load}) \quad (3.8)$$

where in this equation, G_m is the effective trans conductance of the PMOS and NMOS transistors of the back-to-back latch inverters, C_{fn} is the load capacitance at the output of the comparator and ΔV_0 is the initial voltage difference of outputs at $t=t_0$, It can be shown that ΔV_0 can be obtained from,

$$\begin{aligned} \Delta V_0 &= |V_{outp}(t = t_0) - V_{outn}(t = t_0)| \\ &= |V_{Thp}| - \frac{I_{Nt_0}}{C_{Load}} = 2|V_{Thp}| \sqrt{\frac{\beta_{1,2}}{I_{tail}}} \Delta V_{in} \end{aligned} \quad (3.9)$$

After simplifying the equation, the closed-form expression for the power consumption of the dynamic comparator is achieved as below.

$$\begin{aligned} Power_{avg} &= f_{clk} V_{DD} I_{sp1} \left(\frac{1}{8n\phi_t^2} \right) \cdot \tau_{latch} \cdot |V_{Thp}| \times \\ &\quad \left[2k - n|V_{Thp}| + (2k + n|V_{Thp}|) \cdot \exp\left(-2\frac{t_p - t_0}{\tau_{latch}}\right) - 4K \cdot \exp\left(-\frac{t_p - t_0}{\tau_{latch}}\right) \right] \end{aligned} \quad (3.10)$$

Where

$$t_0 = \frac{C_{Load} |V_{Thp}|}{I_{tail} / 2} \quad (3.11)$$

$$t_p = \frac{C_{Load}}{G_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{\Delta V_{in}}\right) \quad (3.12)$$

From the equation derived for the power of double-tail dynamic comparator some vital point can be determined that the power consumption of comparator strongly dependent on the trans-conductance g_m and the leakage power component so by using any method if we decrease either leakage current or trans-conductance or both then we can effectively decrease the power consumption.

Chapter 4:

PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

4.1 Introduction: Due to trans-Conductance (g_m) is greatly effects the power consumption of the comparator a proposed Double-Tail Dynamic Comparator has been define in this chapter. In this literature we will discuss that a small change in circuitry of pre-amplifier stage in dynamic comparator. Placing voltage variable resistor in the discharging path of pre-amplifier stage effect both power consumption and the delay of the circuit. We reduced power of comparator up to a great extent as well as delay of the circuit is also reduced up to some extent. In this chapter also shows the percentage improvement in terms of power consumption, delay, power-delay product (PDP)

Fig. 4.1. Shows the schematic diagram of the proposed double-tail dynamic comparator

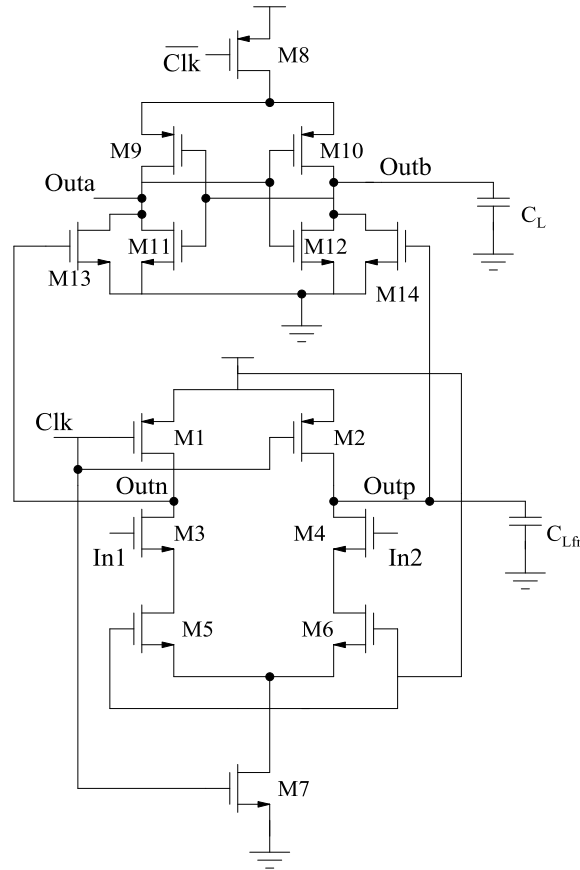


Fig. 4.1. schematic diagram of the proposed double-tail dynamic comparator

Due to well performance in terms of high speed and low power at low voltage application the proposed comparator is designed. To reduce the power of comparator the main concept comes from the conventional circuit that decrease the value of overall trans-conductance g_{eff} . Due to

adding of negative feedback the effective value of trans-conductance g_{eff} decreases up to a great extent. For this purpose two transistor have been added in circuit.

4.2 Operation of the proposed circuit:

The operation of proposed circuit as follows (see Fig. 4). During reset phase (i.e. $\text{clk}=0$) both pMOS M1 & M2 are in conducting stage and pulls the node outa & outb to V_{DD} . The M7 nMOS is in cut off mode so there is no path to discharge for both outa & outb.

During the decision making phase (i.e. $\text{clk}=V_{DD}$) both pMOS come in cut off stage and there is no direct connection between V_{DD} and pMOS and outa and outb nodes start discharging according to the inputs IN1 & IN2. In the proposed circuit M5 & M6 gate is directly connected to the V_{DD} . So both nMOS always in the triode or linear region and act as a voltage variable resistor and both resistance value depend on drain to source voltage (V_{DS}). Discharging of outa & outb is also depending on the voltage variable resistor M5 & M6. If $\text{IN1} > \text{IN2}$ then outa node discharge rapidly then outb node and the resistance of M5 is also low compare to the resistance of M6 so voltage difference between outa node and outb node is greater compare to the conventional double tail dynamic comparator. This voltage difference goes to the latch stage so at any instant M11 comes in cut off stage while at this time M12 is in conducting stage so outp node connected to the ground but outp node now charging from the V_{DD} . So using latch regeneration one node goes to V_{DD} and another goes to ground.

Fig.4.2 shows the output of the double tail dynamic comparator. In the fig. it can be easily seen that In evaluation phase both outp and outn node discharge and according to this decision making phase started. So one of them outa and outb node goes to high and another remain in same condition.

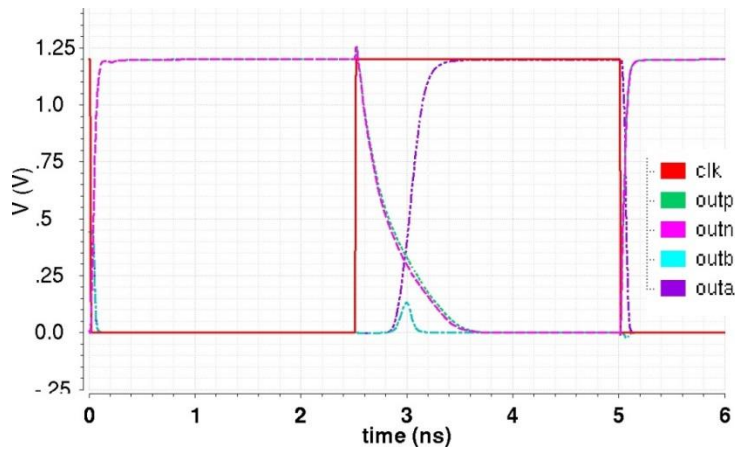


Fig. 4.2. Transient simulations of the proposed double tail dynamic comparator. $V_{DD}=1.2$ V, $\Delta V_{in} = 5$ mV

4.3 Power Analysis:

Power of the comparator hold two main part dynamic power and static power.

$$P_{Total} = P_{Dynamic} + P_{Static} \quad (4.1)$$

Static power analysis: Static power is given by

$$P_{Static} = I_{Leakage} * V_{DD} \quad (4.2)$$

Dynamic power analysis: Dynamic power consists of two part switching power and short circuit power.

$$P_{Dynamic} = P_{Switching} + P_{ShortCircuit} \quad (4.3)$$

Short circuit power $P_{Short\ circuit}$ comes into the picture when clock is switch between either 0 to V_{DD} or V_{DD} to 0 and its value is calculated from [xx].

$$P_{Short} = \frac{K}{12} (V_{DD} - V_{Thn})^3 \frac{\tau}{T} \quad (4.4)$$

Where K is the process parameter, τ is the rise time or fall time of clock signal, T is the time period of clock. Switching power $P_{Switching}$ is a transient power and it is given by

$$P_{Switching} = \int_0^T V_0(t) * I_0(t) \quad (4.5)$$

Now, in order to calculate the power dissipation during the decision-making phase, we notice that I_{supply} is actually the drain current of M5 (see Fig. 3), hence we rewrite equation (6) by inserting the time-variant drain current of M5 according to Tsividis model.

$$Power_{avg} = f_{clk} V_{DD} I_{sp5} \int_{t_0}^{t_p} \ln^2 \left(1 + \exp \left(\frac{V_{DD} - V_{out}(t) - |V_{thp}|}{2n\phi_t} \right) \right) - \ln^2 \left(1 + \exp \left(\frac{V_{DD} - V_{out}(t) - |V_{thp}| - n(V_{DD} - V_{out}(t))}{2n\phi_t} \right) \right) dt \quad (4.6)$$

The integration is performed from the time that regeneration starts (at time t_0) until the end of the regeneration (t_p). In this equation, output voltages are functions of time. In [11] it has been proved that the difference voltage of latch outputs ($V_{outa}-V_{outb}$) changes in a logarithmic manner during the time as follows.

$$\Delta V_{out} = V_{outp} - V_{outn} = \Delta V_0 \exp(G_m t / C_{Load}) \quad (4.7)$$

where in this equation, G_m is the effective trans conductance of the PMOS and NMOS transistors of the back-to-back latch inverters, C_{fn} is the load capacitance at the output of the comparator and ΔV_0 is the initial voltage difference of outputs at $t=t_0$, It can be shown that ΔV_0 can be obtained from,

$$\begin{aligned} \Delta V_0 &= |V_{outp}(t = t_0) - V_{outn}(t = t_0)| \\ &= |V_{Thp}| - \frac{I_{Nt_0}}{C_{Load}} = 2|V_{Thp}| \sqrt{\frac{\beta_{1,2}}{I_{tail}}} \Delta V_{in} \end{aligned} \quad (4.8)$$

After simplifying the equation, the closed-form expression for the power consumption of the dynamic comparator is achieved as below.

$$\begin{aligned} Power_{avg} &= f_{clk} V_{DD} I_{sp1} \left(\frac{1}{8n\phi_t^2} \right) \cdot \tau_{latch} \cdot |V_{Thp}| \times \\ &\quad \left[2k - n|V_{Thp}| + (2k + n|V_{Thp}|) \cdot \exp\left(-2\frac{t_p - t_0}{\tau_{latch}}\right) - 4K \cdot \exp\left(-\frac{t_p - t_0}{\tau_{latch}}\right) \right] \end{aligned} \quad (4.9)$$

Where

$$t_0 = \frac{C_{Load} |V_{Thp}|}{I_{tail}/2} \quad (4.10)$$

$$t_p = \frac{C_{Load}}{G_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{\Delta V_{in}}\right) \quad (4.11)$$

Where

$$G_{m,eff} = \frac{G_m}{1 + G_m r_{ds}}$$

By comparing the expressions derived for the power of the two mentioned structures, it can be seen that the proposed comparator takes advantage of voltage variable resistors in double-tail operation, in two manners which support the whole latch regeneration.

(1) This is due to fact that it gives extra support by using negative feedback in the pre-amplifier stage which decreases the trans-conductance up to a great extent so as the overall power dissipation is effectively decreases.

(2) Since in proposed circuit stacking transistor have been used so leakage current due to DIBL is reduced [9]. Thus overall leakage power consumption also reduced.

Delay analysis of comparator:

It is not only the power analysis which is enhanced in the modified proposed comparator, but the delay is reduced as well. It is improved by using voltage variable resistor which is increase the difference between the input voltages due to both outa and outb node discharge with a different rates. So it will decrease the delay of the comparator by using equation [11]

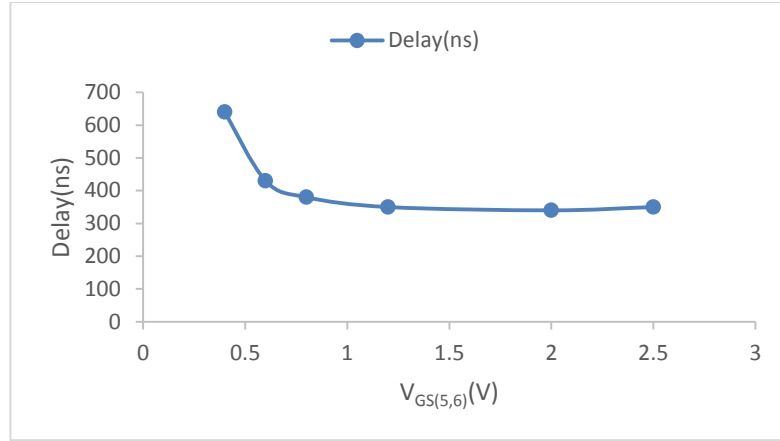
$$t_{delay} = t_0 + t_{latch}$$

$$t_{delay} = 2 \frac{V_{Thn} C_{L,Out}}{g_{m,eff}} \ln \left(\frac{\frac{V_{DD}}{2}}{2 \left(\frac{V_{Thn}}{I_{M5}} \right)^2 g_{mR1,2} g_{m1,2} C_{L,Out} \frac{V_{in1} - V_{in2}}{C_{L,Outb}}} \right)$$

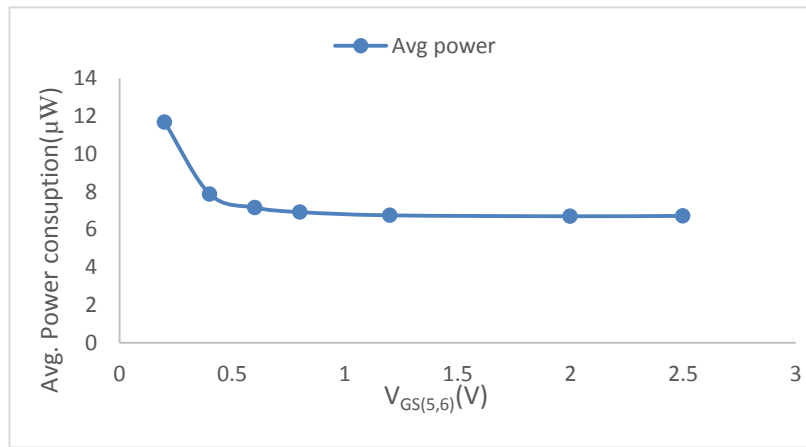
4.5 Design Considerations:

Design of M5 and M6 transistor is very important. If the size of the transistor is high then the delay is reduce due to less leakage current but the power consumption is increase due to area is proportional to power consumption.

Size of the M3 and M4 transistor is also important If the size of M3



(a)



(b)

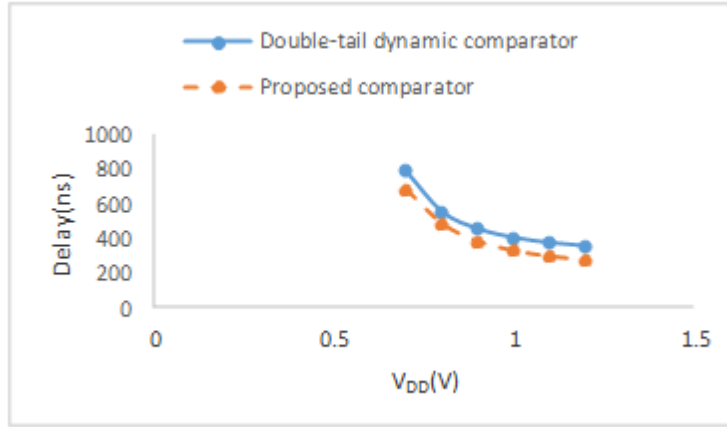
Fig 4.5 Different value of aspect ratio $(W/L)_{5,6}$ V/S (a) Delay (b) Avg. Power Consumption ($\Delta V_{in} = 50$ mV, $V_{DD} = 1.2$ V)

Chapter 5

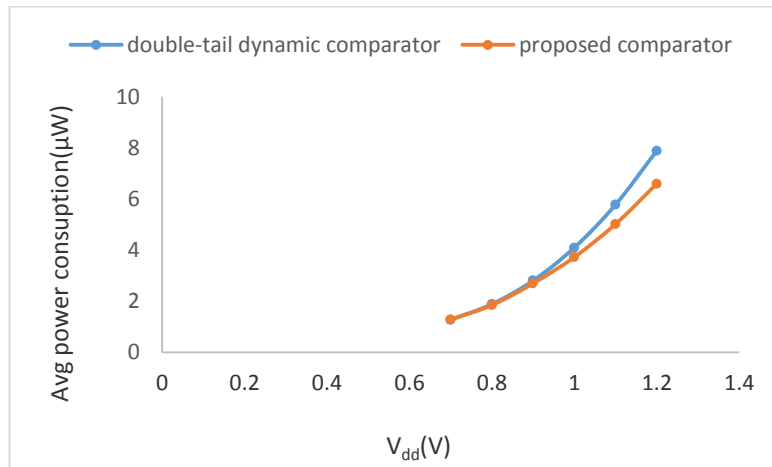
SIMULATION RESULT

In order to compare the proposed circuit with the double tail dynamic comparator all circuit have been simulated in 90 nm CMOS technology with $V_{DD} = 1.2$ V and clock frequency = 200 MHz . Input common mode voltage taken as $V_{cm} = 600$ mV.

Figure 5.1 (a) and (b) shows the post-layout simulation result of the delay and power consumption of the proposed comparator compared with to double tail dynamic comparator. Figure 7 (a) shows the delay of clocked comparators at various bias point of V_{DD} . It is found that at smaller value of V_{DD} (i.e. $V_{DD} = 700$ mV) the percentage improvement is up to 5% and for high value of V_{DD} (i.e. $V_{DD} = 1.2$ V) it is up to 26%. Fig. 5.1(b) shows the avg. power consumption of clocked comparator at various point of V_{DD} . The percentage improvement at lower V_{DD} is given by .7% and the higher power supply the improvement is 16%



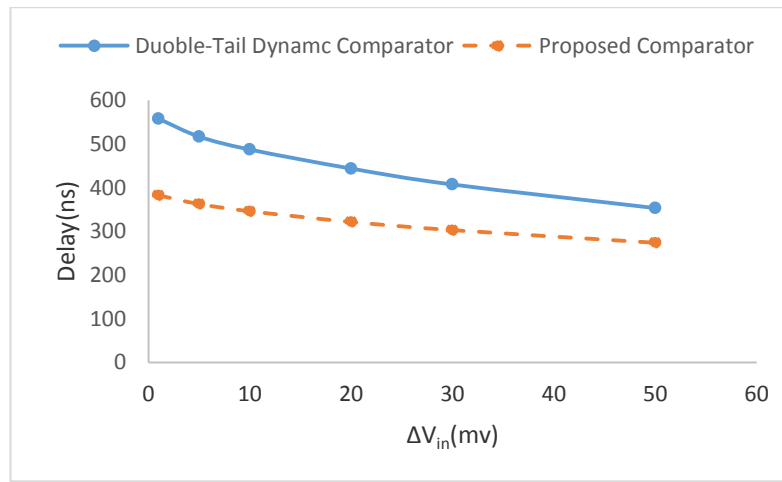
(a)



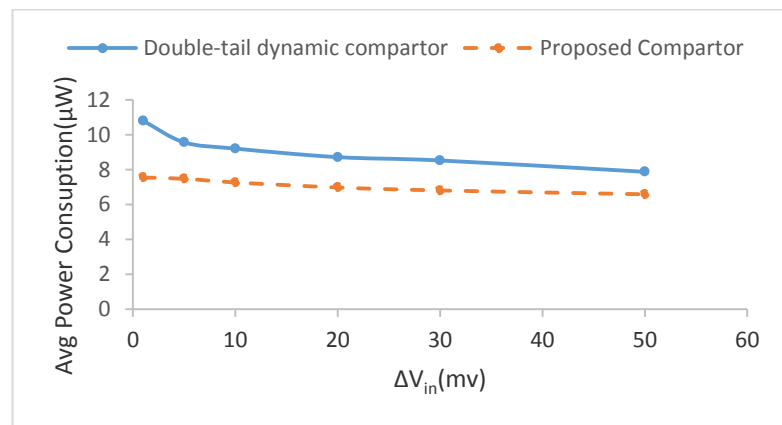
(b)

Fig. 5.1 (a) Post-layout simulation delay and (b) avg. power dissipation as a function of supply voltage ($\Delta V_{in} = 5 \text{ mV}$)

Fig.5.2. Shows various parameter variation at different value of ΔV_{in} . Figure 5.2 (a) displays the comparison between comparators in term of delay at various points of differential voltages. At low value of ΔV_{in} (i.e. $\Delta V_{in} = 1 \text{ mV}$) improvement is 43.1% and at high value of ΔV_{in} (i.e. $\Delta V_{in} = 50 \text{ mV}$) it is found 28.11%. Figure 5.2 (b) shows the comparison between comparators in term of average power dissipation at various bias point of differential voltages. At low value of ΔV_{in} (i.e. $\Delta V_{in} = 1 \text{ mV}$) the improvement is found 30.6% were at high value of ΔV_{in} (i.e. $\Delta V_{in} = 50 \text{ mV}$) it is 16.3%. Due to an improvement in both delay and average power dissipation PDP comes with sound enhancement compared to double tail dynamic comparator.



(a)



(b)

Fig.5.2. (a) Post-layout simulation delay and (b) avg. power dissipation as a function of supply voltage ($V_{DD} = 1.2\text{V}$)

Fig. 5.3 demonstrates avg. power dissipation as a function of ΔV_{in} at different point of V_{DD} . For $V_{DD} = 1.2V$ the avg. power dissipation is $6.59 \mu W$ at $\Delta V_{in}=1mV$. This avg. power dissipation drops from $7.55 \mu W$ to $6.59 \mu W$ when ΔV_{in} changes from $1mV$ to $50mV$.

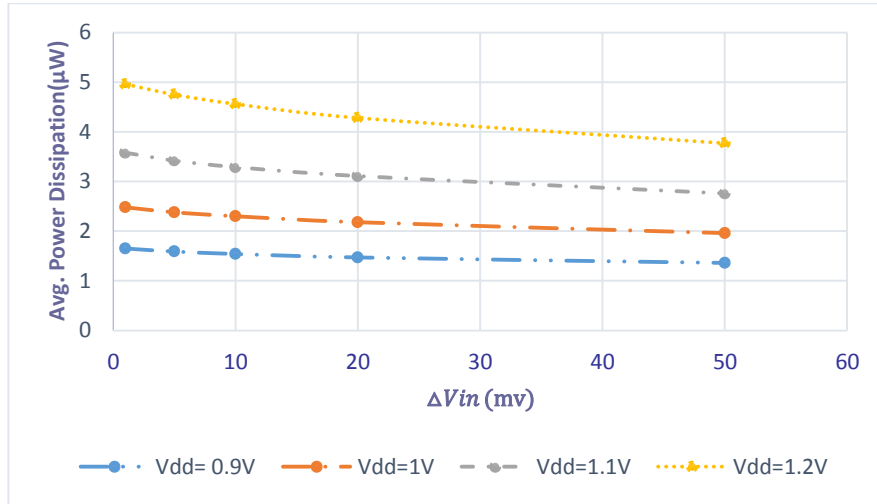


Fig. 5.3. Post-layout simulation of avg. power dissipation as a function of input voltage at various points of V_{DD}

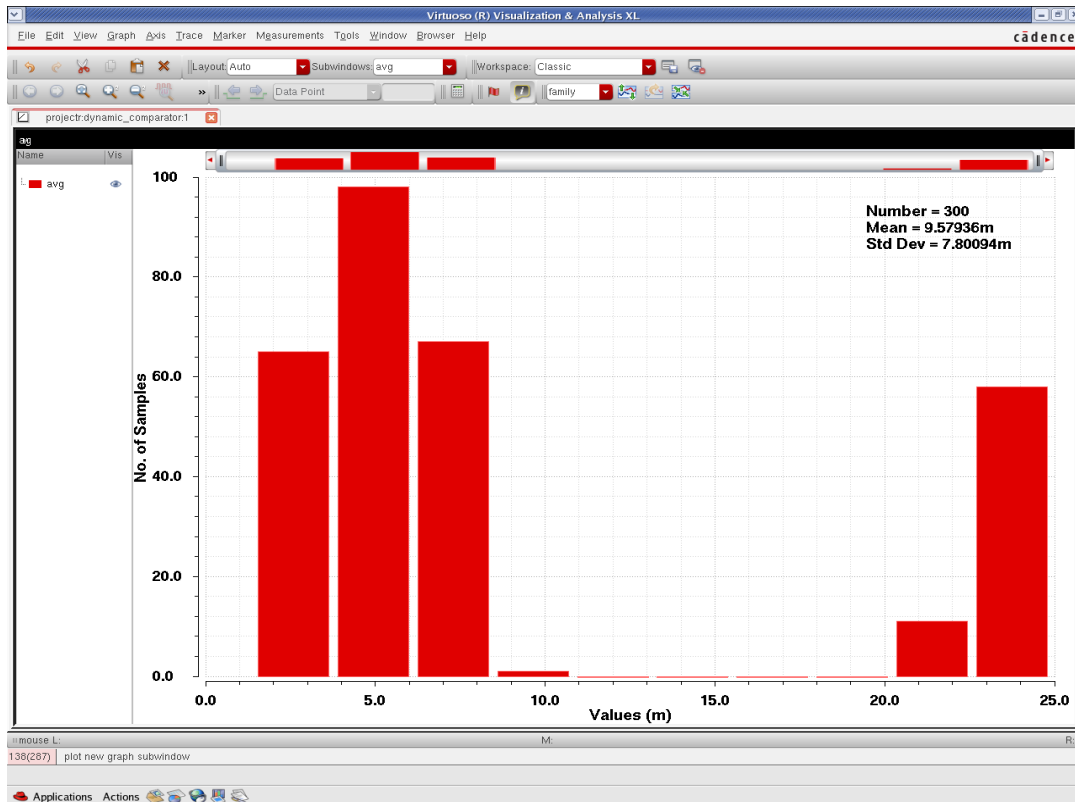


Fig.5.4. Monte Carlo Simulation of input referred offset voltages

Table:1 Comparison between Conventional and proposed double-tail dynamic comparator

Comparator Parameter	Double-tail dynamic comparator [xx]	Proposed Dynamic Comparator	Improvement (%)
Technology CMOS	90nm	90nm	
Supply Voltage (V)	1.2	1.2	
Maximum sampling Frequency	1GHz	1.42GHz	
Delay $/\log(\Delta V_{in})$ ps/dec	273	210	
Avg. power dissipation @ freq. = 200 MHz $V_{in}=50$ mV	7.88	6.59	16.37
PDP (f J)	2.78	1.8	35.25
Input-referred offset voltage(mV)	15.63	7.78	
Estimated Area	$9.3\mu \times 5.6\mu$	$9.3\mu \times 6.0\mu$	

Chapter 6

Conclusion & Future Work

Conclusion:-

To summarize, a double tail dynamic comparator is investigated with source degenerated resistors for the input transistors. Simulation of the proposed comparator shows that it consumes significantly lower power together with higher speed of operation and thereby it results in a significantly lower power-delay product (PDP). In view of the advantages, the propose comparator raises a high possibility of development and implementation of integrated circuits such as ADC with lower power consumption and higher speed of operation.

Future Work:-

In Double-Tail dynamic comparator when we use source degenerated resistors in the input then the total effective g_m is reduced. The effective trans-conductance g_m of the comparator is directly affected the power consumption and the delay of the comparator. Power consumption of the comparator is reduced effetely but the delay of the comparator is increase due to it is inversely proportional to the trans-conductance. So in future

- (1) Reduce the delay up-to great extant
- (2) Increase the dynamic range of comparator
- (3) Increase the ICMR range of comparator

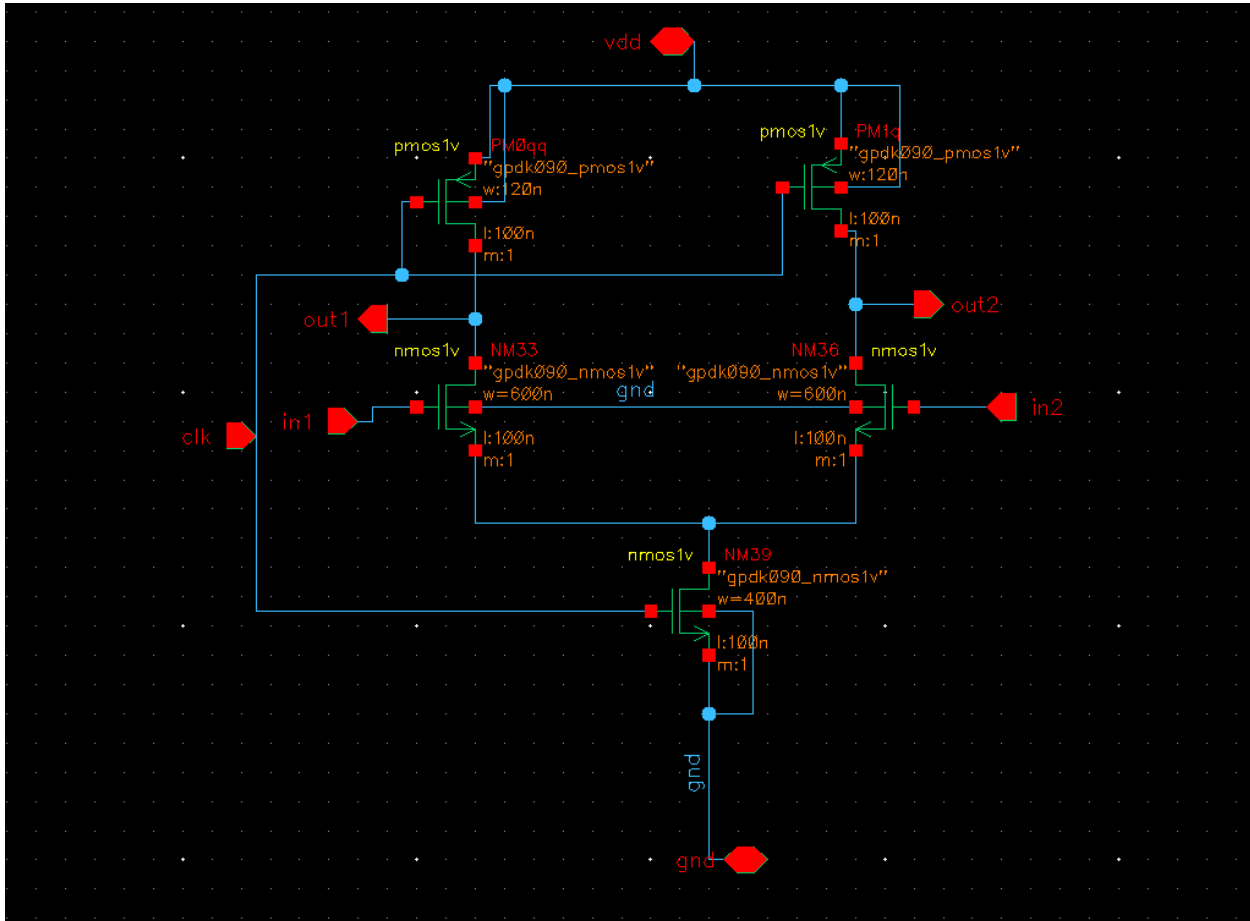
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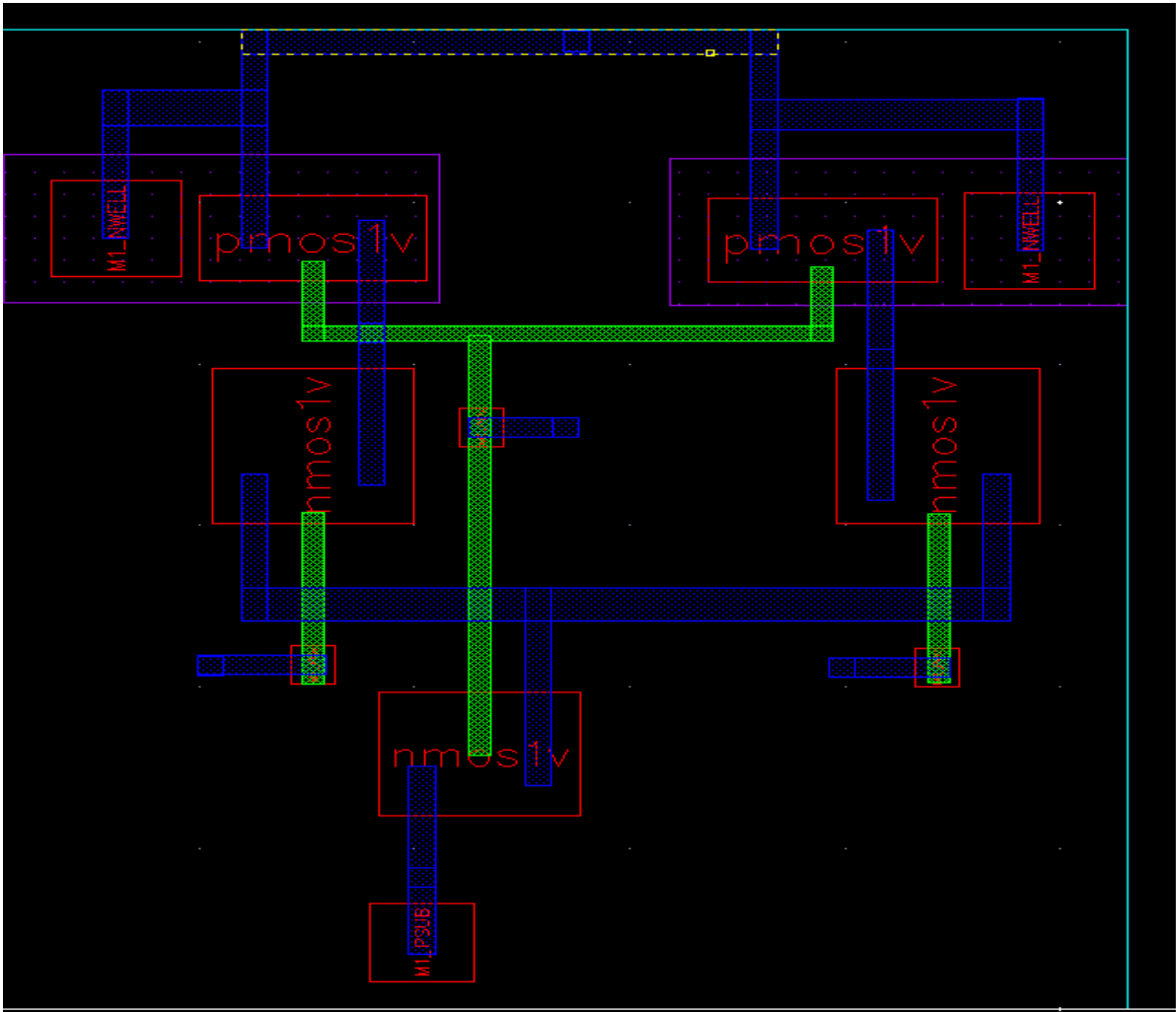
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Appendix

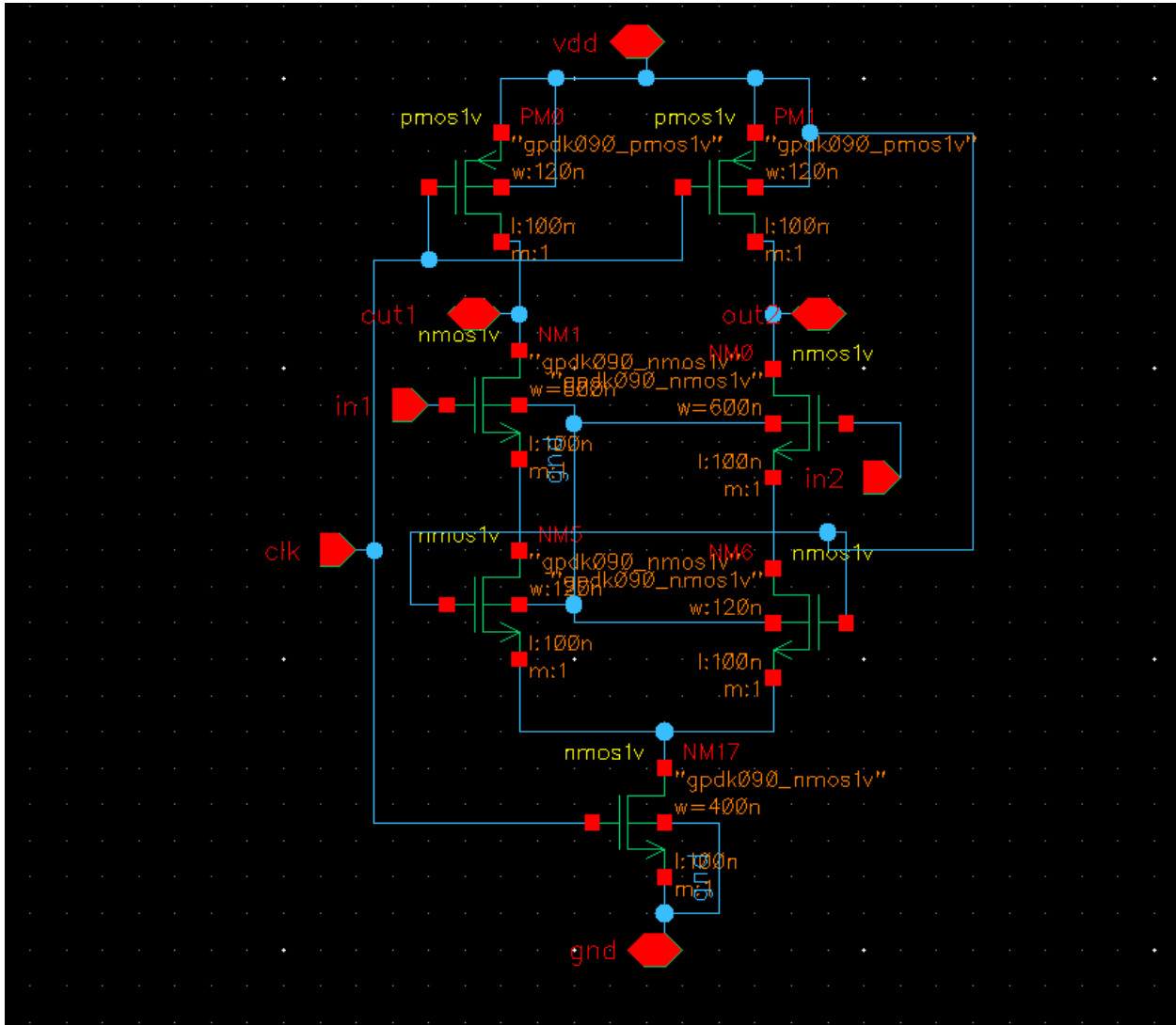
Schematic of Conventional Double-Tail Dynamic Comparator-Input Stage



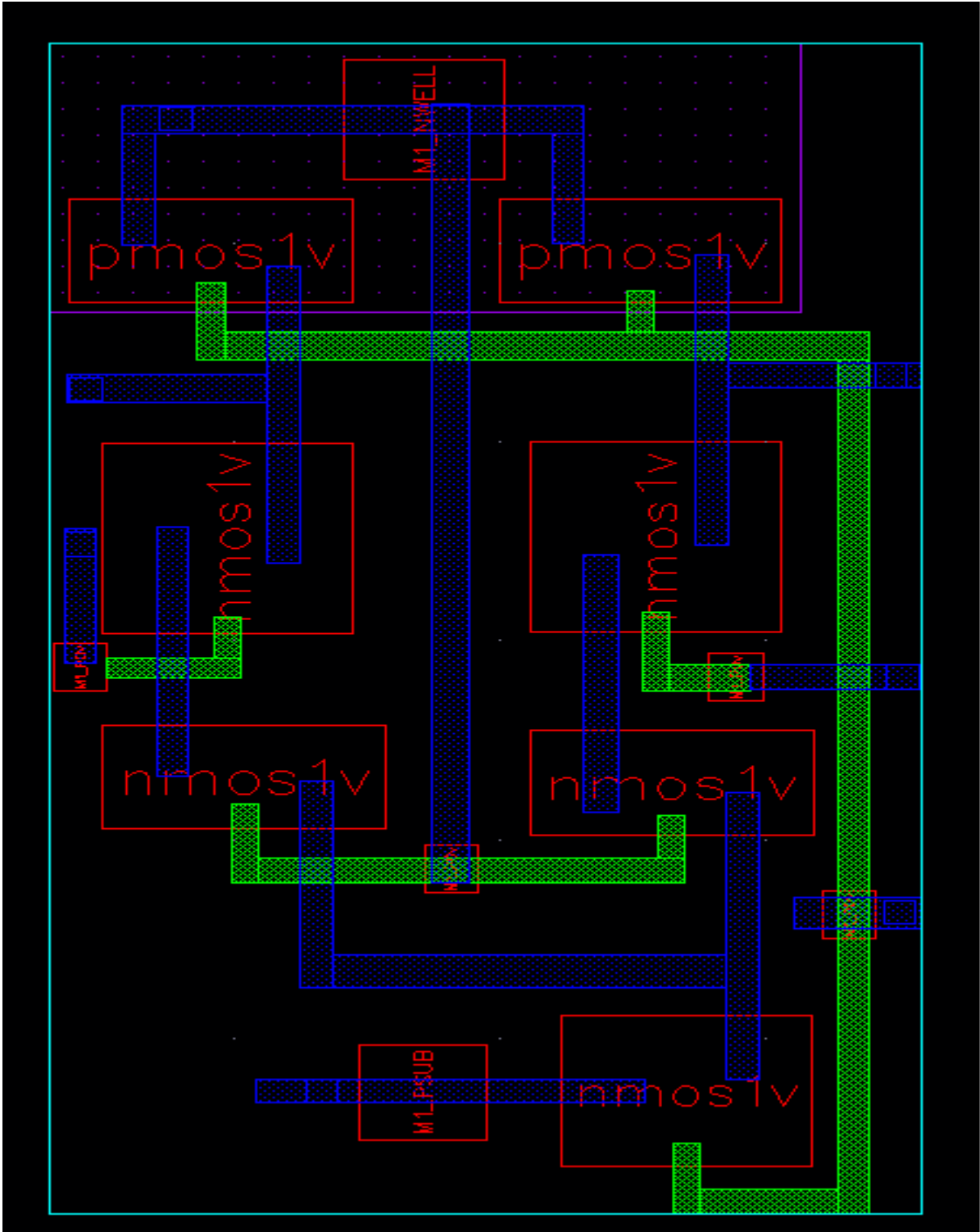
Layout of Conventional Double-Tail Dynamic Comparator-Input Stage



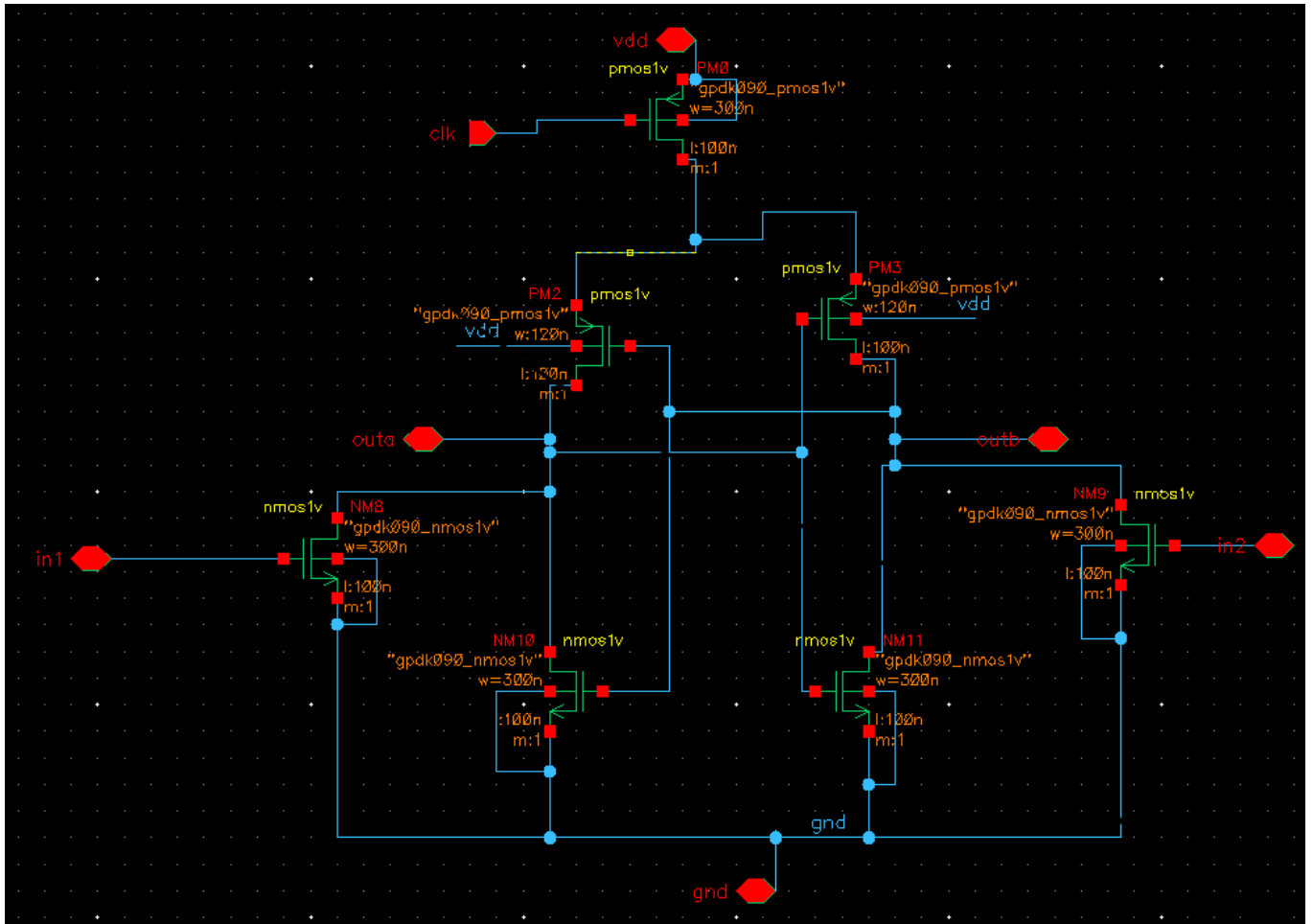
Schematic of Proposed Double-Tail Dynamic Comparator-Input Stage



Layout of Proposed Double-Tail Dynamic Comparator-Input Stage



Schematic of Proposed Double-Tail Dynamic Comparator-Decision Making Stage



Layout of Proposed Double-Tail Dynamic Comparator-Decision Making Stage

